

## CLAIMS

- 1 1. A method for reducing switching activity during a test scan operation of at least one  
2 scan chain in an integrated circuit (IC) comprising the steps of:
  - 3 a) determining stimulus and result value probabilities for a plurality of memory elements in  
4 said IC; and
  - 5 b) connecting said memory elements to form at least one scan chain based on said  
6 probabilities, thereby reducing the switching activity as determined by the probabilities and by  
7 the ordering of said memory elements within said at least one scan chain.
- 1 2. The method of claim 1, wherein said stimulus and result probabilities are determined  
2 by generating and simulating a set of test patterns for said IC.
- 1 3. The method of claim 1, wherein each of said stimulus and result value probabilities  
2 comprise the probability that the stimulus value for a selected memory element coincides with  
3 the result value for said selected memory element.
- 1 4. The method of claim 1, wherein each of said stimulus and result value probabilities  
2 comprise a probability that the stimulus value for a selected memory element is the opposite  
3 of the result value for said selected memory element.

1 5. The method of claim 1, wherein said stimulus and result probabilities comprise for at  
2 least one pair of memory elements whose first element has a stimulus value s1 and a result  
3 value r1 and whose second element has a stimulus value s2 and a result value r2, the  
4 probability that the stimulus value s1 equals s2 and the probability that the result value r1  
5 equals r2.

1 6. The method of claim 5, wherein the probability that said at least one pair of memory  
2 elements will be connected sequentially in at least one of said scan chain increases with a  
3 probability that the stimulus value s1 equals s2 and the result value r1 equals r2, said  
4 probability being computed from said probability that the stimulus value s1 equals s2 and said  
5 probability that the result value r1 equals r2.

1 7. The method of claim 5, wherein the probability that said at least one pair of memory  
2 elements will be connected sequentially in said at least one scan chain increases with a  
3 probability that the stimulus value s1 differs from s2 and the result value r1 differs from r2,  
4 said probability being computed from said probability that the stimulus value s1 equals s2 and  
5 said probability that the result value r1 equals r2.

1 8. The method of claim 3, wherein the probability that at least one pair of said memory  
2 elements will be connected sequentially in said at least one scan chain increases with a  
3 probability that the stimulus and the result values coincide for both elements of said pair, said  
4 probability of stimulus and result values coinciding for both elements of said pair being  
5 computed from said probabilities that the stimulus and result values for each of said memory  
6 elements coincide.

1 9. The method of claim 4, wherein the probability that at least one pair of said memory  
2 elements will be connected sequentially in said at least one scan chains increases with a  
3 probability that the stimulus and the result values are opposite for both elements of said pair,  
4 said probability of stimulus and result values being opposite for both elements of said pair  
5 being computed from said probabilities that the stimulus and result values for each of said  
6 memory elements are opposite.

1 10. The method of claim 5, wherein the probability that at least one pair of said memory  
2 elements will be connected sequentially in at least one of said scan chains decreases with a  
3 probability that the stimulus value s1 does not equal s2 and the result value r1 equals r2, said  
4 probability being computed from said probability that the stimulus value s1 equals s2 and said  
5 probability that the result value r1 equals r2.

1 11. The method of claim 5, wherein the probability that at least one pair of said memory  
2 elements will be connected sequentially in at least one of said scan chains decreases with a  
3 probability that the stimulus value s1 equals s2 and the result value r1 does not equal r2, said  
4 probability being computed from said probability that the stimulus value s1 equals s2 and said  
5 probability that the result value r1 equals r2.

1 12. The method of claim 7, wherein said sequential connection of said pair of memory  
2 elements includes an inversion between said pair of memory elements.

1 13. The method of claim 3, wherein said step of sequentially connecting memory elements  
2 includes sequentially connecting at least one pair of memory elements, said pair of memory  
3 elements being determined by a computing value extracted from the equation:

4 
$$D(A,B) \{ 1 + K [ pm(A)(1 - pm(B)) + pm(B)(1 - pm(A)) ] \}, \text{ wherein}$$

5  $D(A,B)$  is a distance between said pair of memory elements,

6  $pm(A)$  is a probability that said stimulus and result values of a first memory element of said  
7 pair are the same,

8  $pm(B)$  is a probability that said stimulus and result values of a second memory element of said  
9 pair are the same, and

10  $K$  is a constant value.

1 14. The method of claim 1, wherein test patterns are generated for said IC, at least one of  
2 said test patterns including a stimulus value which is undetermined for at least one of said  
3 memory elements, said undetermined stimulus value being set to a value which does not cause  
4 switching during a scan operation between said memory element and the nearest closest  
5 preceding memory element in said chain for which a value was determined by said test  
6 pattern.

1 15. The method of claim 1, wherein test patterns are generated for said IC, at least one of  
2 said test patterns including a stimulus value which is undetermined for at least one of said  
3 memory elements, said undetermined stimulus value being set to a value which does not cause  
4 switching during a scan operation between said memory element and the nearest closest  
5 following memory element in said chain for which a value was determined by said test  
6 pattern.

1 16. The method of claim 1, wherein test patterns are generated for said IC, at least one of  
2 said test patterns including a stimulus value which is undetermined for at least one of said  
3 memory elements and a result value which is determined for said at least one memory  
4 element, said undetermined stimulus value being set to coincide with said determined result  
5 value.

1 17. The method of claim 1, wherein test patterns are generated for said IC, at least one of  
2 said test patterns including a stimulus value which is determined for said at least one memory  
3 element, a result value which is undetermined for said at least one memory element, and  
4 stimulus values which are undetermined for at least another memory element, and wherein at  
5 least one of said undetermined stimulus values is set to a value which causes said  
6 undetermined result value to have a value that coincides to said determined stimulus value.

1 18. The method of claim 5, wherein said sequentially connecting said pair of memory  
2 elements is determined by computing a value determined by the equation:

3 
$$D(A,B) \{ 1 + K [ ps(1 - pr) + pr(1 - ps) ] \}, \text{ wherein}$$

4  $D(A,B)$  is a distance between said pair of memory elements,  
5  $ps$  is said probability that  $s_1$  equals  $s_2$ ,  
6  $pr$  is said probability that  $r_1$  equals  $r_2$ , and  
7  $K$  is a constant value.

1 19. The method of claim 1, wherein a set of test patterns is generated for said IC, at least one  
2 pair of members of said test pattern set are merged to reduce the number of elements in said  
3 set of test patterns, a total switching activity during scan-in of said merged pattern is  
4 computed, and said merging is rejected if said computed total switching activity exceeds a  
5 predetermined limit.

1 20. The method of claim 1, wherein a set of test patterns is generated for said IC, a total  
2 switching activity during scan-out of result values for at least one member of said test pattern  
3 is computed, and said test pattern is rejected if said total computed switching activity exceeds  
4 a predetermined limit.

1 21. The method of claim 2, wherein a maximum switching activity during scan-in or scan-out  
2 of any test pattern of said set of test patterns is determined for at least one candidate scan  
3 chain ordering, said candidate scan chain ordering being rejected if said maximum switching  
4 activity exceeds said predetermined limit.

1 22. A method of reducing the switching activity during a test scan operation of at least one  
2 scan chain in an integrated circuit (IC) comprising the steps of:

3 a) generating a set of test patterns for said IC, comprising values that include at least one  
4 stimulus value for at least one memory element and at least one result value for another of  
5 said at least one memory elements;

- 6 b) determining from at least one of said test patterns at least one probability of coincidence  
7 between at least one pair of said values;
- 8 c) connecting said at least one memory element and said at least another memory element to  
9 form at least one scan chain based on said at least one probability; and
- 10 d) setting undetermined stimulus values in said test patterns to values that minimize  
11 switching activity during a scan operation based on the order of said memory elements  
12 connected in step c).

1 23. A program storage device readable by a machine, tangibly embodying a program of  
2 instructions executable by the machine to perform method steps for reducing the switching  
3 activity during a test scan operation of at least one scan chain in an integrated circuit (IC), the  
4 method steps comprising:

- 5 a) determining stimulus and result value probabilities for a plurality of memory elements in  
6 said IC; and
- 7 b) connecting said memory elements to form at least one scan chain based on said  
8 probabilities, thereby reducing the switching activity as determined by the probabilities and by  
9 the ordering of said memory elements within said at least one scan chain.